Embedded Test Processors (ETP)

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ABSTRACT

This paper describes a versatile methodology to implement controlled built in self test (BIST). It makes use of an embedded test processor architecture and it supports the use of different design for test (DFT) methods. This BIST methodology can be reused, at any time, during the designs entire life cycle time. The test application time at the PCB (Printed Circuit Board) or MCM (Multi Chip Module) level is reduced if circuits used has both Boundary Scan (BS) and this BIST methodology implemented. Synthesis of the test strategy can be performed.

INTRODUCTION

Integrated circuits, as digital ASIC's, FPGA's and standard circuits, are becoming more and more complex. The number of gates on each chip are increasing rapidly, so also the number of pins. The number of gates are growing faster than the number of pins, this gives that the number of gates hidden behind each pin is increasing all the time.

The clock frequencies used on the digital circuits are also increasing. µProcessors for computers is a good example of this development. The µPr version 386 was available in the frequency ranges 20-40 MHz. The next version of this µPr family, the 486, is available in the frequencies 20-66 MHz and with the different options as DX2, DX3 and so on. Now is the Pentium available, the lowest clock frequency manufactured is 70 MHz and the highest clock version available, for the moment, is 166 MHz and higher clock frequency versions are to come.

This trend in higher complexity and higher functional speed is creating new demands not only on design methodology but also on how to perform design for testability (DFT). Already today are the bigger circuits, as high performance µPr's designed by many design engineers working in parallel. To keep the total design time as short as possible , the implementation of the test functions must be just as modular as the implemented functionality. With an ETP, modular testing is fully supported.

The trend in higher and higher clock frequencies, it makes it necessary to run the test at the same speed as during normal operation. Full speed test is the only strategy that makes it possible to detect all delay faults. By using a test structure based on an ETP, the test(s) can run at normal operating speed by using BIST for all the different parts of a design.

THE EXISTING TEST METHODOLOGIES

The traditional view of test, it is a procedure only performed during the manufacturing phase. The test methodologies developed, and used, with this approach are:

- Internal Scan (SCAN)
- Boundary Scan (BS) 1149.1
- Built in self test (BIST)
- I_{DDQ}

All these four methodologies can be used in conjunction with an external tester. Backtracks with using an external tester to carry out the different tests are:

- The two first types of tests are performed at a limit clock speed, normally in the range 1-10 MHz.
- I_{DDQ} is performed at even lower speed.
- BIST can be executed at the frequency used during normal operation, this as long as supported by the tester used.
- The traditional testers are normally very expensive, about 1 MUSD, and they can't be moved out in the field.
- It is difficult to reuse the embedded test structures at the PCB/MCM level, this since most of the methodologies either need a high degree of interaction with the outside world or/and a non standardised communication is used.

To be able to also detect "delay faults" during testing, it is getting more and more important to be able to run the tests at operational speed, this is supported by BIST and

also SCAN (if internal stimuli and response generators are embedded on the silicon).
Only the methodology BS is designed in such a way that it supports hierarchical test, this through the standardised Test Access Port (TAP) interface [6] [8].

HOW TO PERFORM HIERARCHICAL TEST

Due to the increased complexity of integrated circuits and also PCB's/MCM's, it is getting more and more important to be able to reuse the implemented TEST methodologies during both the circuits, PCB/MCM and systems entire life-time. This introduce the demand to be able to easily access the tests performed at the circuit level also at the PCB/MCM and system level. This can only be achieved if more or less all parts of the tests implemented at the circuit level are totally embedded in the circuit and a standard interface can be used to both activate the tests and read the results from the tests. One proposal on how to perform such a solution [3] is according to the figure to follow.

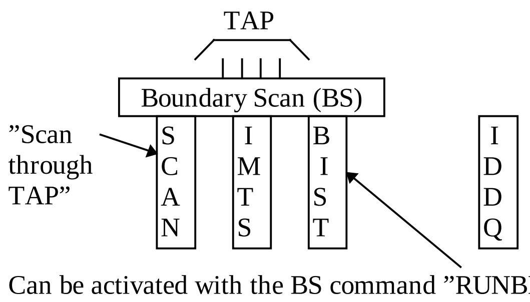

Fig. 1 All tests performed through the TAP, prop. 1.

IMTS stands for "Inter-Module Test Structures" and is the hardware structure that interconnects and carries out the different test methodologies. As can also be seen from figure one, I_{DDQ} is not that easy to incorporate in this structure.
The proposal in figure one can be improved by using an ETP instead of an IMTS, this as described in the figure to follow.

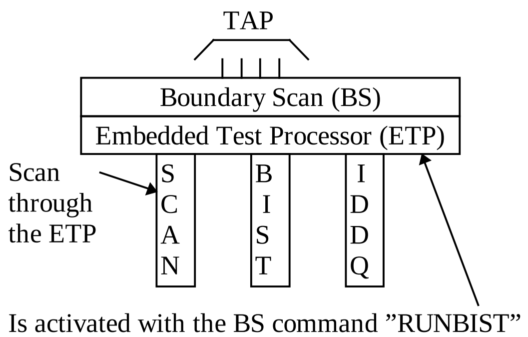

Fig. 2 All tests performed through the TAP, prop. 2.

With this proposal, the command to start to perform a test of the entire circuit is always activated by performing the boundary Scan command "RUNBIST". This makes the activation of test of the circuit totally transparent to the internal design of the circuit and is independent of the number of blocks with BIST and internal SCAN that is implemented.
A test of type I_{DDQ}, it can be performed if the comparator to sense the power consumption current is embedded in the circuit. The ETP can be used to setup the internal logic blocks with the logical levels needed. During the measurement, the ETP shall go into a low (or known) power consumption level or its power consumption shall not be measured by the comparator.
The ETP approach has the benefit that it is possible to easily reuse the tests at the IC level also at the PCB/MCM level. This due to that a minimal level of activity is needed through the serial BS interface. The small level of activity needed through the serial BS interface, it both reduces the total test time and also adds a minimal amount of work to create test programs at the PCB/MCM level. A board test controller (BTC) [9] at the PCB/MCM level can be used to connect the PCB/MCM, from test point of view, with the sub-system. The BTC can be used to carry out high level commands from the subsystem as test commands to the ETP(s) and other parts of the PCB/MCM.

THE PROCEDURE TO CARRY OUT A BIST ON BLOCKS WITH HIGH DENSITY STRUCTURES

Independently of if the BIST is for functional block of type a RAM ROM, PLA or other type of regular logic, the procedure to carry out a BIST can always be the same. A complete command procedure can be in the order from top to bottom as:

- Activate the test by setting a signal "run" to logical high.
- As soon as the test is recognised as running, set the signal "run" to logical low again.
- When the BIST is ready, read the signature of the result flag(s) from the block.

This procedure is repeated for all blocks with BIST.

THE PROCEDURE TO CARRY OUT A BIST ON BLOCKS WITH LOW DENSITY STRUCTURES

This type of blocks are normally tested by connecting the D flip-flops into Scan chains. To be able to use the ETP to carry out an internal Scan of different functional user blocks, the blocks should have a structure as described in the figure to follow.

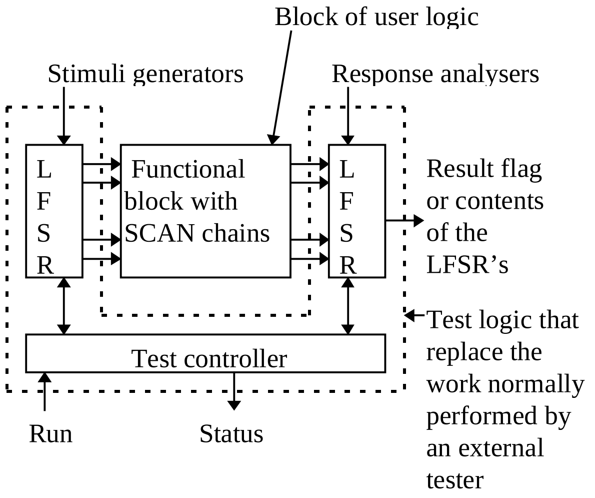

Fig. 3. SCAN test controlled by the ETP.

The procedure to carry out an internal SCAN is always the same. A complete command procedure can be in order from top to bottom as:

- Set up the algorithm to be used in the LFSR's
- Set up the number of test-vectors to be executed.
- Activate the test by setting a signal "Run" to logical high.
- As soon as the test is recognised as running (Status=1), set the signal "Run" to logical low again.
- When the test is ready (Status=0), read the signature(s) or the result flag(s) from the block.

This procedure is repeated for all blocks. The 1st and 2nd step (of the five) are included to make it possible to run the total test as a set of sub tests. To perform the total test with as high fault coverage as possible by using a minimal number of test vectors, each sub-test can run with different algorithms and for different number of test vectors. This approach makes it possible to create "ready to use" LFSR blocks. The size of a LFSR block can be selected by using a "size parameter" or they can have a fixed size. The creation of the test logic structure, to control a scan based BIST, can be part of a test synthesis operation [7]. Such an incorporation would make it possible to automatically generate inputs needed for the program controlling the function of the ETP.
LFSR's generate random, or almost random, test patterns for the functional block being tested. These patterns are more effective for burn-ins and environmental stress testing than typical patterns written for system test or diagnostics purposes, because random and almost random patterns tend to exercise the logic to its fullest extent [10].

DESIGN CONSIDERATIONS FOR AN ETP

For some years ago it was a big difference between designing an ASIC and a µPr. Today is more or less all µPr designers using the same standard tools as used for ASIC designs. The conclusion is that it is no problem to design a general µPr block dedicated for test.
Shall an ETP be created with an µPr of the type CISC (Complex Instruction Set Computer) or a RISC (Reduced Instruction Set Computer) ? A RISC is preferred due to that it will have a smaller physical size and also a simpler structure [4] [5], this without any significant loss in performance.
During normal operation, the activity level of a circuit is between 1 and 5% [1]. To avoid thermal stress during test, the total activity level during test must be taken into consideration. Since activities as BIST and internal SCAN creates a high level of activity, only parts of the circuit can be tested at the same time when running the tests at operational speed. If the ETP is only used to start and analyse tests of different blocks, there is no need that the ETP is running at higher clock frequencies as 20-40 MHz. This gives that the same design of an ETP can be used for different circuit designs, this independent of the actual speed of the system clock used by the circuit. Even if the ETP is running at a lower clock frequency than the functional blocks in a circuit, the increase in the total test time can be expected to be limited. This due to that:

- Only one or a few functional blocks can run in test mode at the same time, this to avoid thermal stress.
- Setup and preparation of the next set of block to run in test mode, this can be performed while other blocks are running in test mode.

This means that it is possible to design an ETP as a general ready to use block or a set of ready to use sub blocks that either can be selected by hand by the design engineers or selected with a special test tool. This test tool should be part of the development environment, this in the same way as the SCAN insertion function is part of the synthesis tools used today. The creation of the program that controls the function of the ETP, it should be created with special test tool that work together with tools such ATPG (Automatic Test Pattern Generator) tools.

TEST AT POWER-ON OR RESET

It is essential to know that the ETP is working properly before it can be used to carry out test(s) on the different functional blocks in the circuit. An automatic test of the ETP must be performed every time a power-on or reset occur. The test must be of the type BIST. The result from the test of the ETP must be saved in an internal register, the register must be readable through the BS interface. This readable register must also include a status information telling if the test is ready or running.
At the same moment as the test of the ETP is ready and no faults are found, an internal test of all the functional blocks in the circuit can be performed.
The ETP can easily be configured to automatically perform a full or partial test of the circuit every time it is

powered up and/or at end of a reset of the circuit. This gives a good possibility to test that the startup behaviour of the circuit is as expected. Since the tests can run at operational speed, the total time to perform such startup test is limited to a minimum.

EXPECTED SIZE OF AN ETP

There exist already a few (ready to use) µPr designs, intended to be used as an embedded µPr, on the market. Example of such processors are the ARM processor from VLSI Technology Inc. [4] and the µRISC [2] from NORDIC VLSI AS. The µRISC is a µPr designed as 4 bit slices, where a slice can be used to create a 4, 8, 12 or 16 bit µPr. The µPr has a Harvard architecture and has a total of 31 instructions where most of the instructions execute in one clock cycle. The different blocks in the µRISC has embedded BIST functions. The µPr is designed to work with an operation frequency in the range 0 to 40 MHz. The total number of general purpose registers are 16 and it can use 64 I/O addresses. An 8 bit ALU core of the µPr and in a 1 µm process has the physical size as defined in the table to follow. The width of the ROM is 16 bits and the width of the RAM is 8 bits.

ROM (words)	RAM (bytes)	Area (mm^2)
1024	64	3.3
2048	128	4.4
4096	192	6.2

Table. 1. Sizes of a µRISC with different ROM and RAM sizes

The processes used in a near future can be expected to have an size of 0.5 µm or less. This gives that the total size of an ETP can be expected to be very small. It may also be possible to use less than 31 commands in an ETP, this may make it possible to use a ROM with a width less than 16 bits.

CONCLUSIONS

An ETP will have a small physical size. It can be used to setup, start and read the results of BIST for the different user blocks in a circuit. As long as it is not involved in the execution of the BIST for different blocks, the ETP can run on a fixed frequency, for example 40 MHz, and still can the BIST for the different blocks execute at the operation frequency (this even if the operational frequency, for the user logic, is 200 MHz or higher). The ETP can be designed as a ready to use standard block. If the BS interface 1149.1 is used as an interface to the outside world, the tests executed by the ETP can easily be reused at PCB/MCM or even system level. Since the level of activity needed through the BS interface is limited, the amount of work to write the test program to activate the ETP and read the results form the tests carried out by the ETP are limited.

ACKNOWLEDGEMENT

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